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Description

[STRUCTURE OF QUANTUM DOT LIGHT EMITTING DIODE AND METHOD OF FABRICATING THE SAME]

Cross Reference to Related Applications

[0001] This application claims the priority benefit of Taiwan application serial no.92105988, filed on March 19, 2003.

Background of Invention

[0002] Field of the Invention

[0003] The present invention relates to a structure of InAs/GaAs quantum dot light emitting diode and a method of fabricating the same, and more particularly to a structure of nano-technology light emitting diode and a method of fabricating the same that can improve sensitivity thereof.

[0004] Description of the Related Art

[0005] Traditionally, the method of forming epitaxial structure is performed by a self-organized mold. Because of difference of material surface energy, the energy creates stress

thereon, and the material tends to form a low-dimension crystal shape, such as an island. If a new structure is to be formed, the material property can be applied in the method for forming the structure. In some structures, the periodic variations on the surface of the material, a grain structure can be formed. In three-dimension structure, a crystal structure can be formed because of the stress. Generally, the epitaxy of hetero interface includes three modes Frank-vanderMerwe disclosed in 1949, Volmer-Weber disclosed in 1926 and Stranski-Kranov disclosed in 1937, wherein Stranski-Kranov mode is most popularly used. Traditionally, a cracking valve should be deposed between As shutter of an epitaxial apparatus for forming quantum dot structure. The modification of the epitaxial apparatus, however, costs a lot for changing the As source system of the original epitaxial apparatus.

SUMMARY OF INVENTION

[0006] An InAs/GaAs quantum dot light emitting diode is disclosed. InAs/GaAs quantum dot light emitting diode which is formed by turning off an As shutter and using As background concentration for epitaxy, comprises a Si-doped GaAs substrate, a N-type structure, an undoped quantum well, a quantum dot layer, a spacer layer, a barrier layer

and a P-type structure. The undoped quantum well can reduce the mobility of carriers within the epitaxial structure and enhance the probability of recombination of electrons and holes, the efficiency of luminescence is, therefore, improved.

Brief Description of Drawings

[0007] FIG. 1 is a schematic drawing for showing an epitaxial structure.

[0008] FIG. 2 is a schematic process flow of forming the quantum dot light emitting diode.

[0009] FIG. 3 is electroluminescence measurements of the device varying with temperatures.

Detailed Description

[0010] FIG. 1 is a schematic drawing for showing an epitaxial structure.

[0011] Please referring to FIG. 1, a (001)±1° Si-doped GaAs substrate 1, which has a thickness about from 320 μm to about 380μm and dopant concentration from about 1×10^{18} to about 1×10^{19} cm^{-3} is provided. A GaAs buffer layer 2 having a thickness about from 500 nm to about 2000 nm and dopant concentration from about 1×10^{18} to about 5×10^{19} cm^{-3} is formed on the substrate 1 when substrate

temperature is about from 580 to about 615°C. Then, a $Al_xGa_{1-x}As$ cap layer 3 having a thickness about from 200 nm to about 800 nm and dopant concentration from about 1×10^{18} to about 5×10^{18} cm^{-3} is formed on the GaAs buffer layer 2, wherein x is about 0.3-0.7 when substrate temperature is raised to 610°C to about 650°C. Two to ten multi-layer GaAs /undoped $Al_xGa_{1-x}As$ quantum wells 4 then are formed on the cap layer 3, wherein each quantum well has a thickness about from 3 nm to about 7 nm, and x is about 0.3-0.7 when substrate temperature is down to 580°C to about 615°C. Three to ten InAs quantum dot mono layers 5 then are formed on the quantum wells 4, wherein each quantum dot mono layer has a thickness from about 2.5 mono layer (ML) to about 4.5 ML, when substrate temperature is down to 470°C to about 520°C. Then each quantum dot layer is covered with an undoped GaAs spacer layer 6 having a thickness from about 10 nm to about 40 nm. Then, a GaAs barrier layer 7 having a thickness from about 10 nm to about 50 nm is formed on the last spacer layer 6. The InAs quantum dot layer 5 is formed by using an As background concentration in a MBE chamber for epitaxy when an As shutter is turned off, wherein the growth rate of the InAs

quantum dot layer 5 is about 0.05-0.5 ML/sec. Then a $Al_xGa_{1-x}As$ cap layer 8 having a thickness from about 300 nm to about 700 nm is formed on the GaAs barrier layer 7, wherein x is about 0.3-0.7 and Be concentration is from about 1×10^{18} to about 1×10^{19} cm^{-3}. Finally, a GaAs contact layer 9 having a thickness from about 300 nm to about 1000 nm is formed on the cap layer 8, which is doped with Be having concentration from about 5×10^{18} to about 5×10^{19} cm^{-3}, and the structure of the quantum dot light emitting diode is complete.

[0012] FIG. 2 is a schematic process flow of forming the quantum dot light emission diode.

[0013] A silicon-doped GaAs substrate 10 having an N-type structure 11, a quantum dot layer 12 and a P-type structure 13 sequentially formed thereon is provided at step S14. Then a photoresist coating step S15 is performed. A photolithographic step S16, an etching step S17, a photoresist removing step S18, a silicon oxide deposition step S19 and a photoresist coating step S20 are then sequentially performed. Then an photolithographic hole step S21, a silicon oxide etching step S22, a photoresist removing step S23, and a photoresist coating step S24 are sequentially performed. A metal deposition step S25, an Au/Be

alloy deposition step S26, a lift-off step S27 and a substrate grinding as well as an Au/Ge alloy deposition on the backside of the substrate S28 are sequentially performed.

[0014] FIG. 3 is electroluminescence measurements of the device varying with temperatures, wherein relative Intensity and wavelength show in the curve 40 which represents EL curve at 10^{o}K, the curve 41 represents EL curve at 60^{o}K, the curve 42 represents EL curve at 120^{o}K, the curve 43 represents EL curve at 180^{o}K, the curve 44 represents EL curve at 240^{o}K, andthe curve 45 represents EL curve at 300^{o}K.

[0015] An InAs/GaAs quantum dot edge light emitting diode with the peak emission wavelength of 1μm is disclosed. The shift of peak wavelength is about 0.22 nm/K under 20~300 K. The temperature-dependent broadening of full width at half maximum (FWHM) of electro-luminescence (EL) spectrum is 0.04 nm/K.

[0016] Strained layer epitaxy is an effective method for fabricating self-assembled zero dimensional (0D) InAs / GaAs quantum dots. The 7 % lattice mismatch between the epitaxial InAs and GaAs layers is performed by Stransky-Krastanov growth mode. The device was grown by solid-source molecular beam epitaxy. When temperature is from

about 20 to 300 K, the dark current is reduced from 84 pA to 13 nA at the negative bias of - 0.5 V. The ideality factor is abruptly down from about 14 (tunneling current is dominant) at 20 K down to 2 (G-R current) at the range of 100 to 240 K, then approaches to about 1.3 (diffusion current) smoothly. That means that the device has a low dark current and excellent diode electric performance. In addition, the position of peak wavelength is changed from 0.99 to 1.05 μm due to energy gap shrinkage of semiconductor when increase of temperature. Under the operation during the very large temperature range, the wavelength shift and the broadening FWHM are only 0.22 and 0.04 nm/K, respectively. These results are comparable with resonant cavity LED and the LED with the surfacing multiplayer dielectric optical filter. The intensity versus current (L-I) characteristics is essentially linear during the temperature range. The equivalent threshold currents are generated by the parallel constant current leakage path varying with temperature. The slopes of L-I decrease with the increase of temperature.

[0017] Although the present invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be con-

structed broadly to include other variants and embodiments of the invention which may be made by those skilled in the field of this art without departing from the scope and range of equivalents of the invention.